1/8/9

ATTORNEY'S DKT No. APPLICATION NO. H1132 <del>Unassig</del>ned **INFORMATION** APPLICANT(S) 26615 DISCLOSURE Ming-Ren Lin et al. PATENT TRADEMARROYFICE FILING DATE GROUP CITATION Unassigned PTO-1449 July 8, 2003 **U.S. PATENT DOCUMENTS EXAMINER'S FILING** SUBCLASS PATENT NO. DATE CLASS **INITIALS** NAME DATE FOREIGN PATENT DOCUMENTS Translation **EXAMINER'S** DATE COUNTRY **CLASS** SUBCLASS INITIALS PATENT NO. No OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) Digh Hisamoto et al., "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," TEEE Transactions on Electron Devices, Vol. 47, No. 12, December 2000, pages 2320-2325. Yang-Kyu Choi et al., "Sub-20nm CMOS FinFET Technologies," 2001 IEEE, IEDM, pages 421-424. Xuejue Huang et al., "Sub-50 nm P-Channel FinFET," IEEE Transactions on Electron Devices, Vol. 48, No. 5, May 2001, pages 880-886. Xuejue Huang et al., "Sub 50-nm FinFET: PMOS," 1999 IEEE, IEDM, pages 67-70. Yang-Kyu Choi et al., "Nanoscale CMOS Spacer FinFET for the Terabit Era," IEEE Electron Device Letters, Vol. 23, No. 1, January 2002, pages 25-27.

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).